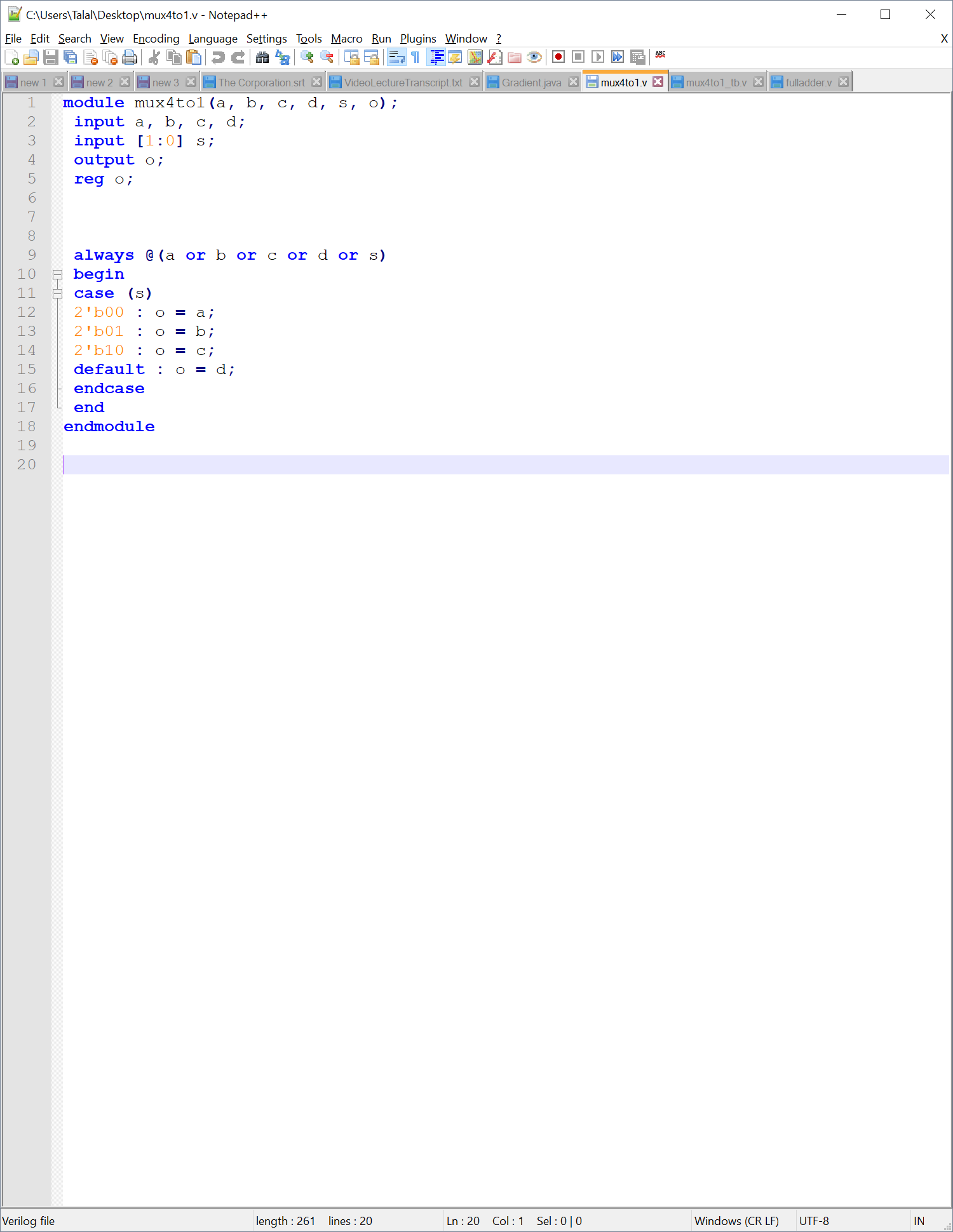
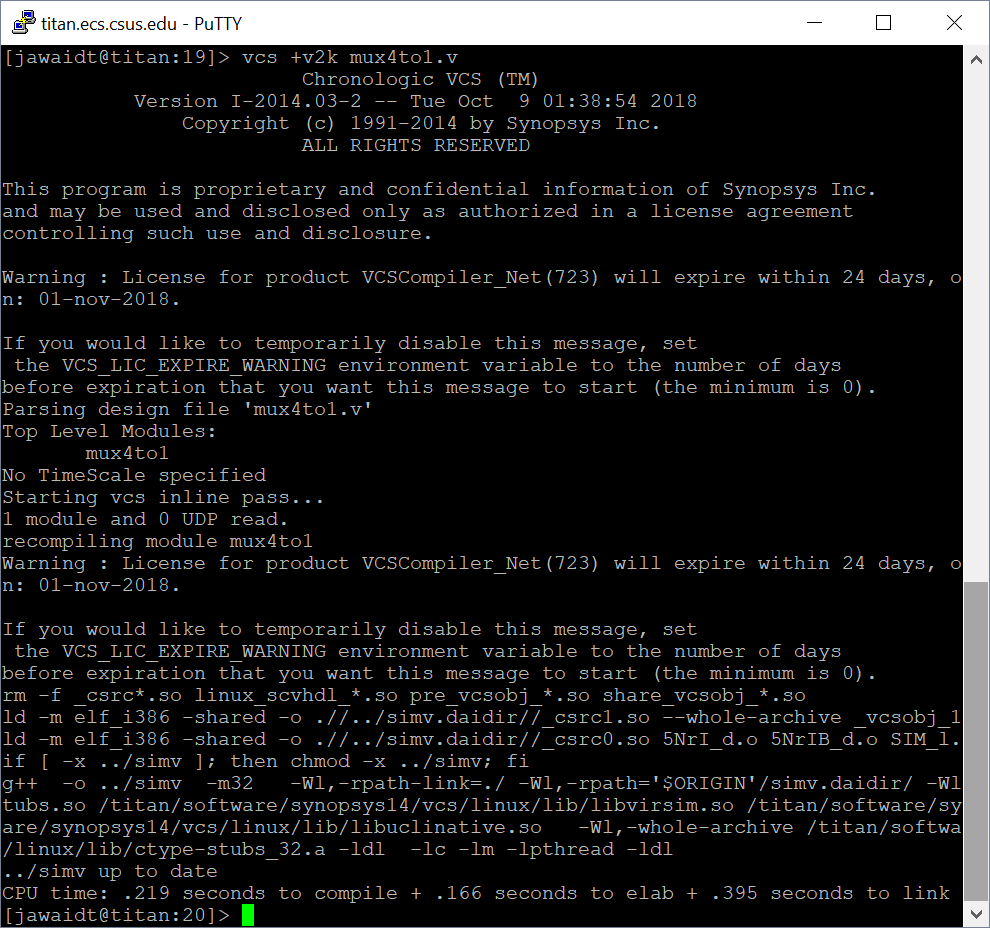
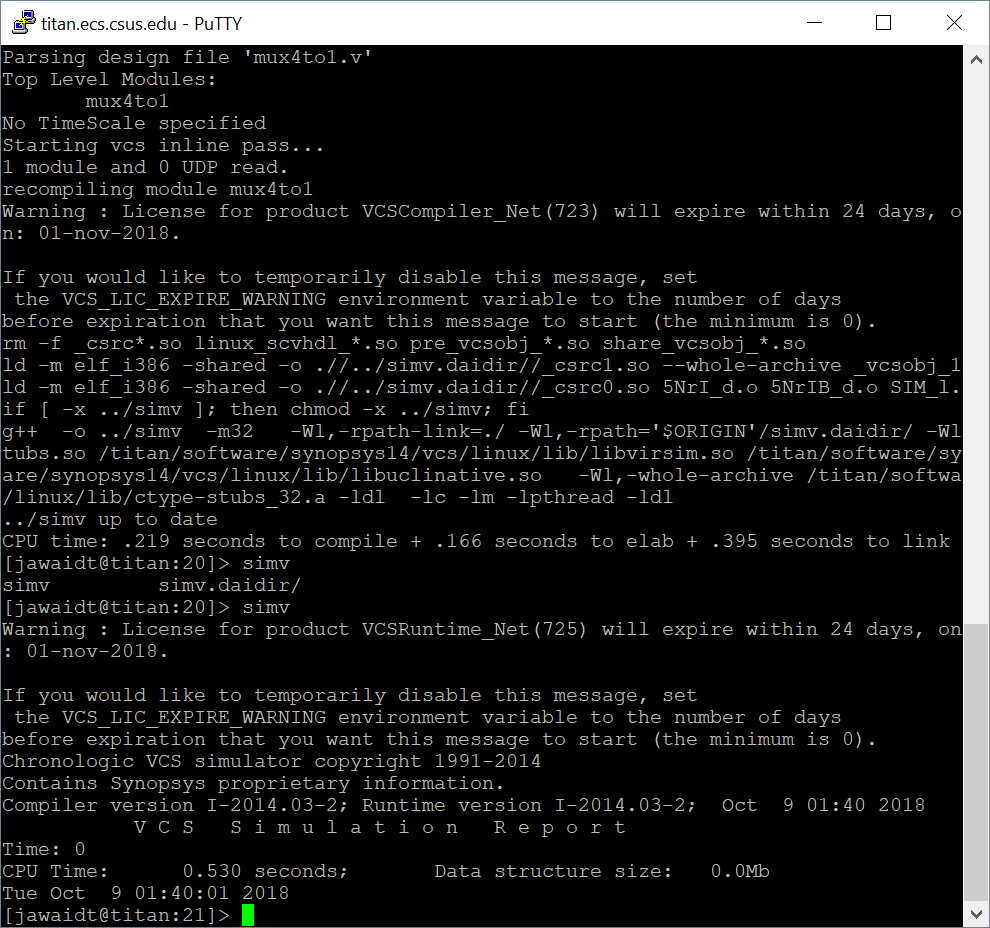
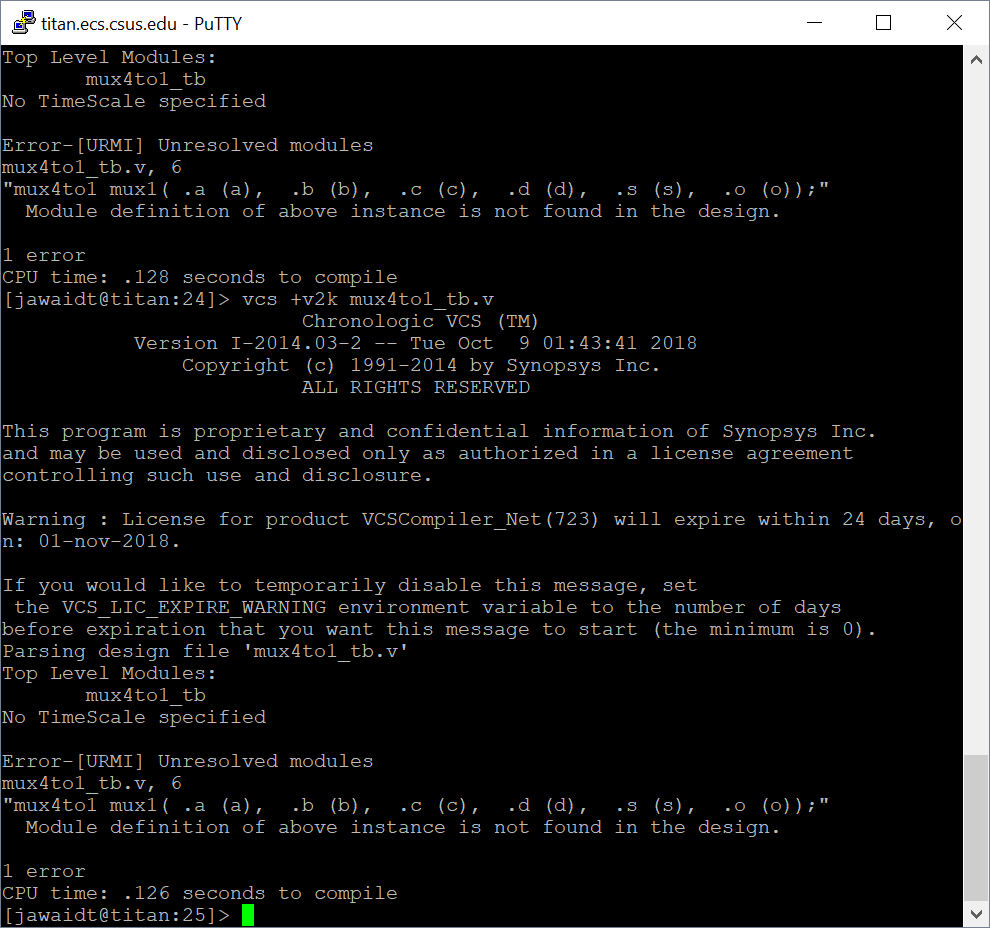
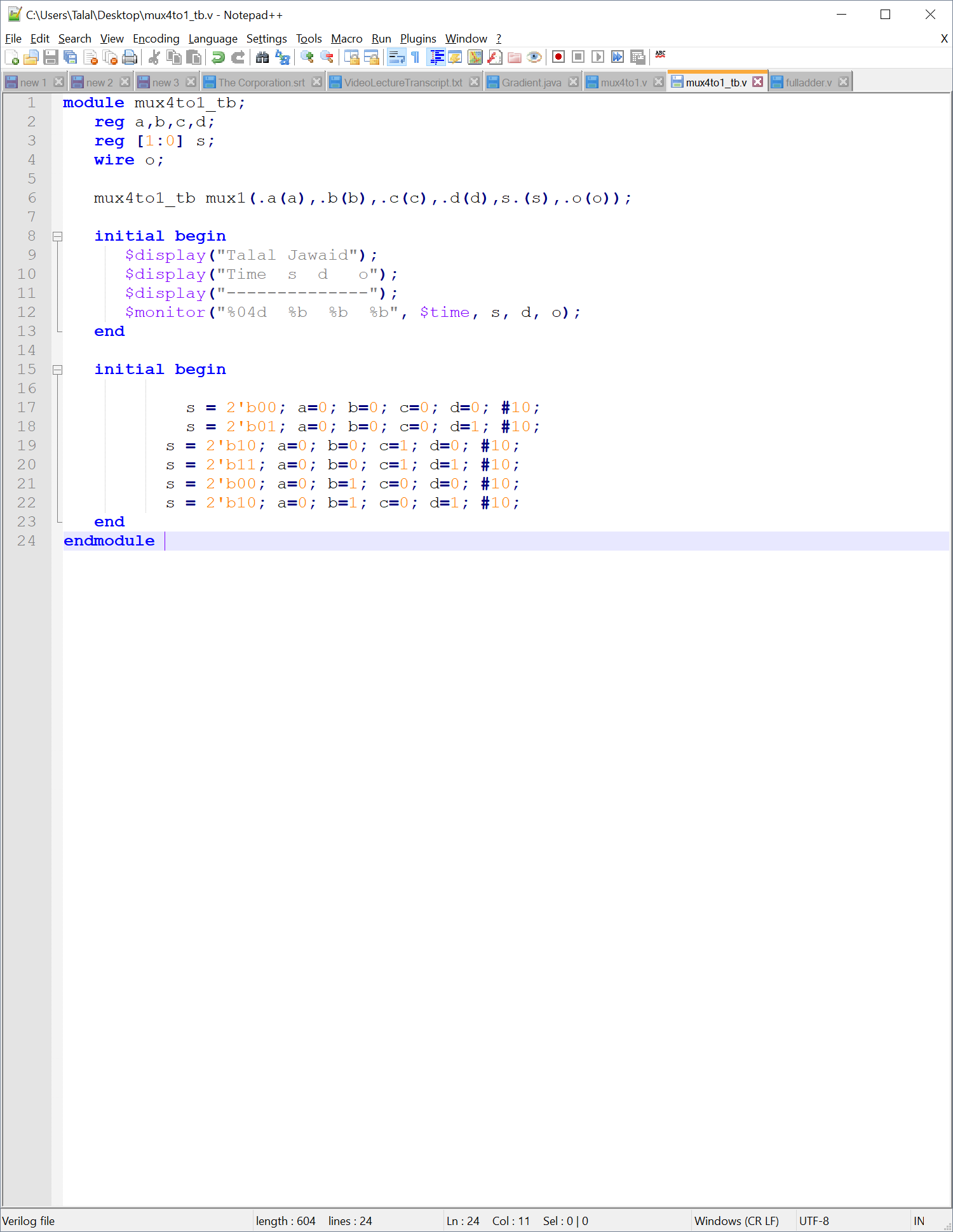
4x1 Multiplexer 

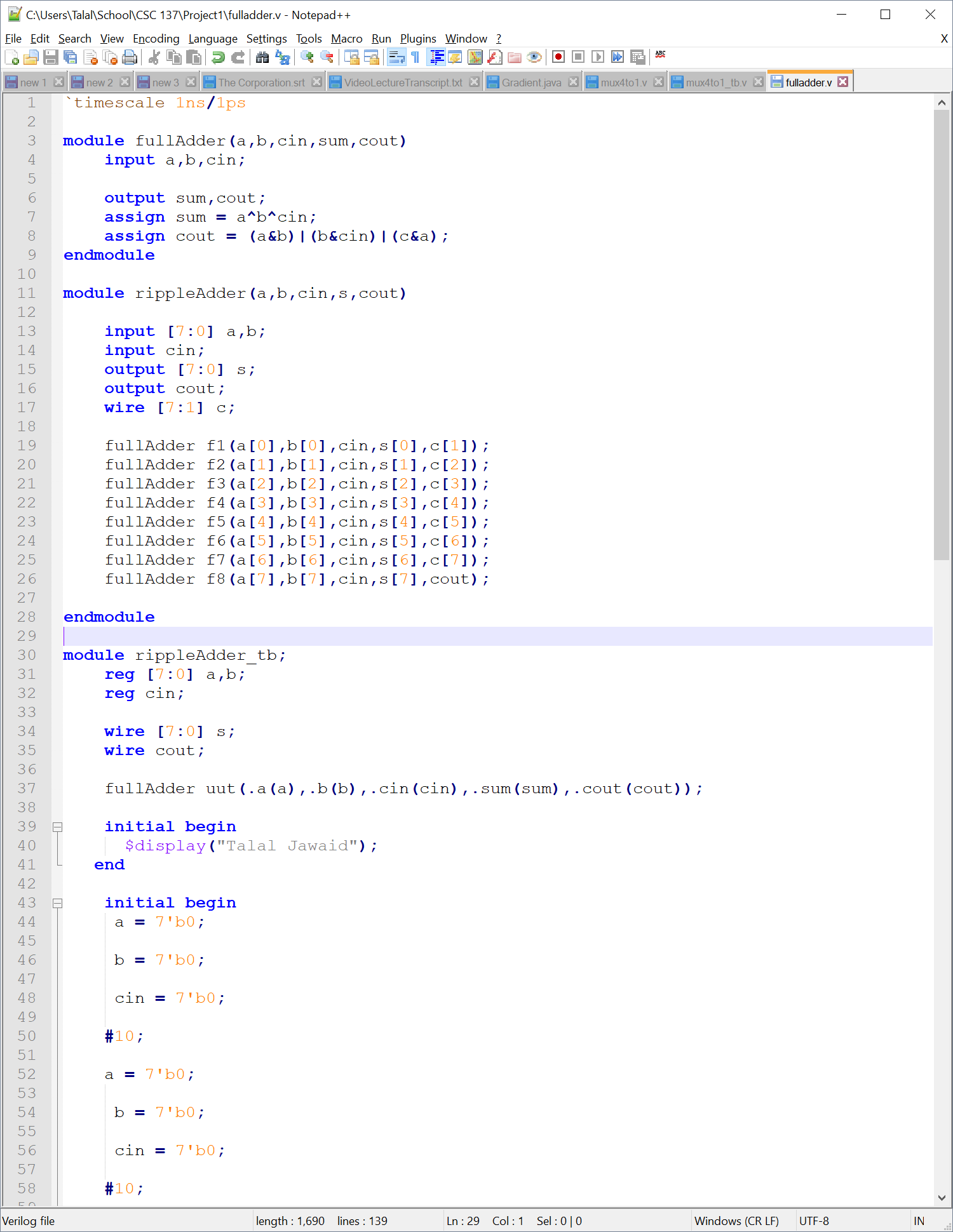
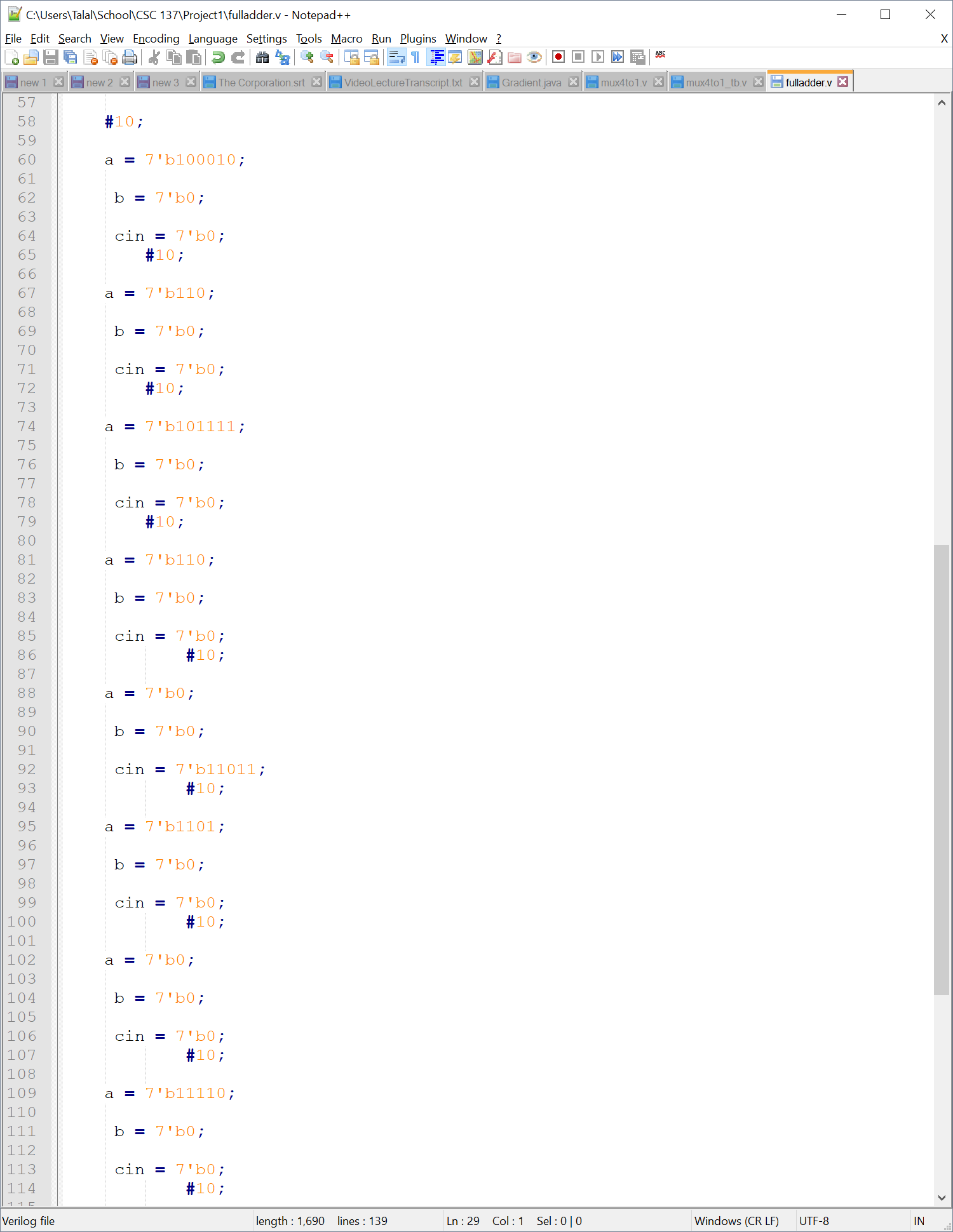
Attempting to compile

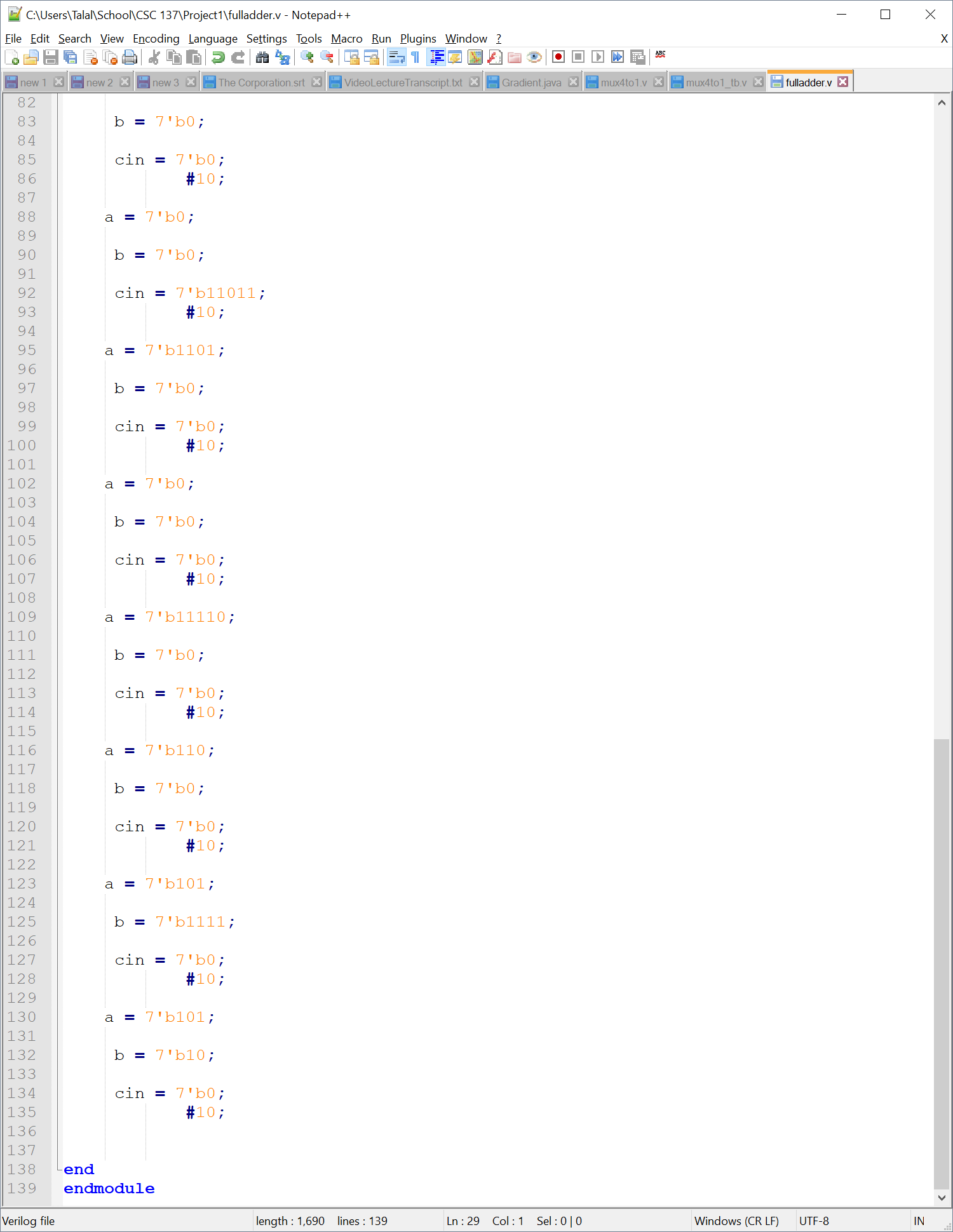


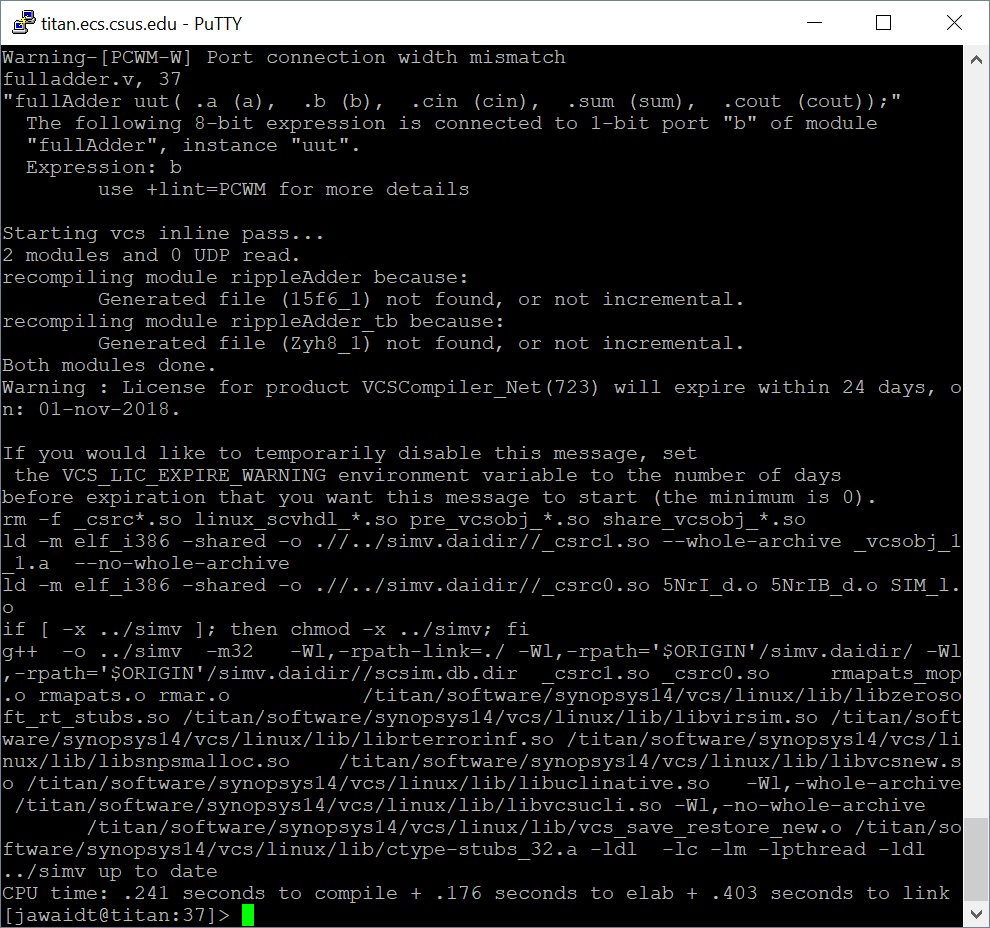
Attempting to run via simv

Attempting to compile mux4to1\_tb

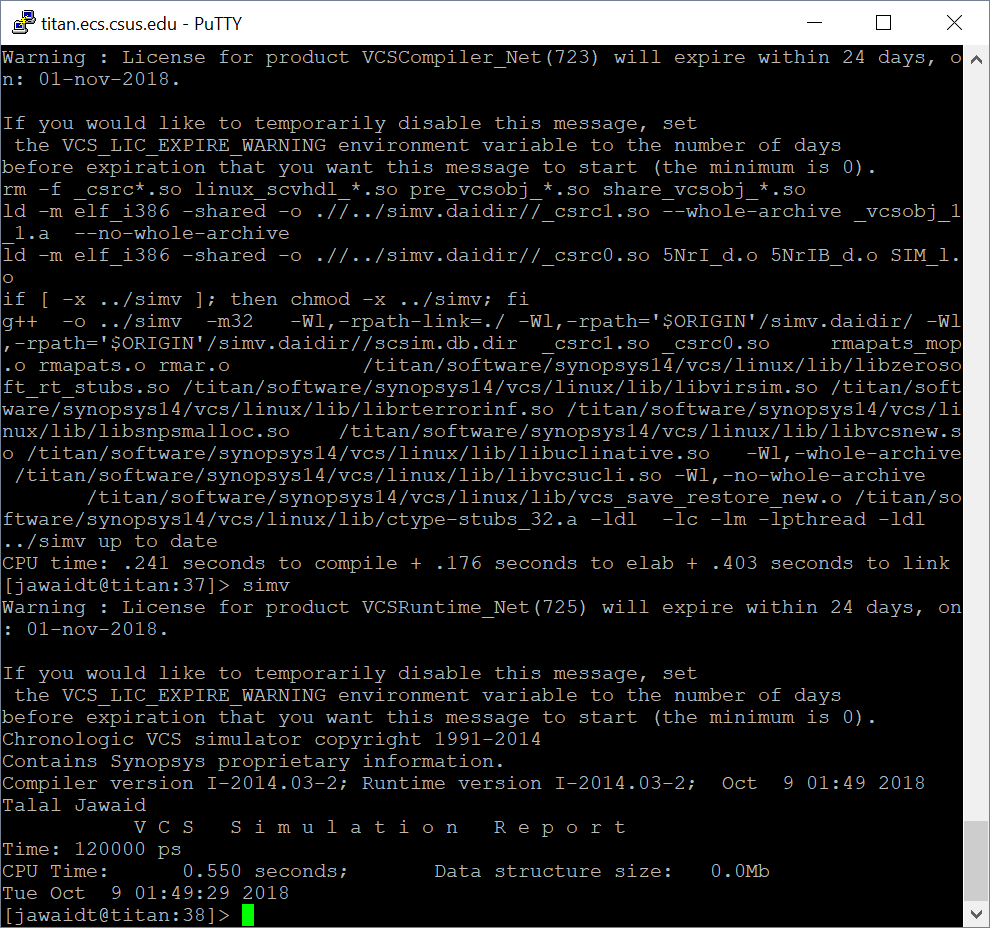
4x1 Multiplexer test bench

Full Adder, 8 bit ripple carry adder, test bench 





Compiling fulladder.v



Attempting to run via simv

All files compiled, synthesized, and ran through Quartus and Vivado. Not sure why VCS and SIMV weren’t working. Test benches did not correctly work in Quartus or Vivado.